CLAIMS

1. A method of storing data in a dynamic random access memory ("DRAM") device in either a normal operating mode when the DRAM device is active or a power-saving mode when the DRAM is inactive, the method comprising:

in the normal operating mode, refreshing memory cells in the DRAM device at a first rate; and

in the power-saving mode, scrubbing the memory cells in the DRAM device at a second rate that is substantially less than the first rate.

2. The method of claim 1 wherein the act of scrubbing the memory cells in the DRAM device at a second rate comprises scrubbing the memory cells in the DRAM device at a rate that is a function of the temperature of the DRAM device.

3. The method of claim 1 wherein the act of scrubbing the memory cells in the DRAM device at a second rate comprises scrubbing the memory cells in the DRAM device at a rate that is initially a function of the temperature of the DRAM device and is thereafter adjusted as a function of the number of memory errors that are found to exist in a prior memory scrubbing procedure.

4. The method of claim 1 wherein the act of scrubbing the memory cells results in correcting any memory errors that may exist in the DRAM device, and wherein the act of scrubbing the memory cells in the DRAM device at a second rate comprises scrubbing the memory cells in the DRAM device at a rate that is a function of the number of memory errors that are found to exist in a prior memory scrubbing procedure.

5. The method of claim 4 wherein the act of scrubbing the memory cells in the DRAM device at a rate that is a function of the number of memory errors that are found to exist comprises:

increasing the rate if the number of memory errors is greater than a predetermined value; and

decreasing the rate if the number of memory errors is less than a predetermined value.

6. The method of claim 1 wherein the act of scrubbing the memory cells in the DRAM at a second rate comprises:

sequentially scrubbing the memory cells from a first row to a last row of a memory array in the DRAM device; and

after scrubbing the last row of the memory array, waiting for a delay period corresponding to the second rate before repeating the sequential scrubbing of the memory cells from the first row to the last row of the memory array in the DRAM device.

7. The method of claim 1 wherein the act of scrubbing the memory cells in the DRAM at a second rate comprises:

sequentially scrubbing the memory cells from a first row to a last row of a memory array; and

after scrubbing each row of memory cells, waiting for a delay period corresponding to the second rate before scrubbing another row of memory cells.

8. The method of claim 1 wherein the act of scrubbing the memory cells in the DRAM device comprises:

reading data from the memory cells of the DRAM device;

reading check bits associated with the data from the DRAM device;

generating check bits from the read data;

generating a syndrome from the generated check bits and the read check bits; and

in the event the syndrome indicates there is an error in the read data and/or check bits, generating corrected data and/or check bits, and writing the corrected data and/or check bits to the memory cells of the DRAM device.

9. The method of claim 8 wherein the act of writing the corrected data and/or check bits to the memory cells of the DRAM device comprises:

combining the corrected data and the check bits to provide a corrected ECC; and

writing the corrected ECC to the DRAM device.

10. The method of claim 8 wherein the act of writing the corrected data and check bits to the memory cells of the DRAM device comprises:

writing the corrected data to a first location in the DRAM device; and

writing the corrected check bits to a second location in the DRAM device that is separate from the first location.

11. A method of operating a dynamic random access memory ("DRAM") device in a power-saving mode, comprising:

reading a set of data bits from each of a plurality of groups of memory cells in the DRAM device;

generating a respective set of check bits corresponding to each of the sets of data bits read from each group of memory cells;

storing the sets of check bits in the DRAM device;

after a delay, reading each set of data bits and corresponding sets of check bits from the memory cells;

generating a set of syndrome bits derived from each of a respective set of data bits read from the DRAM device and from the corresponding set of check bits read from the DRAM device;

determining from each of the sets of syndrome bits if any of the respective set of read data or read check bits is in error;

if the syndrome indicates any bits of the read data is in error, correcting the error to generate corrected data;

if the syndrome indicates any of the check bits is in error, correcting the error to generate corrected check bits;

writing any corrected data to the DRAM device; and

writing any corrected check bits to the DRAM device.

12. The method of claim 11 wherein the delay is a function of an operating characteristic of the DRAM device.

13. The method of claim 12 wherein the delay is a function of the temperature of the DRAM device.

14. The method of claim 12 wherein the delay is initially a function of the temperature of the DRAM device and is thereafter adjusted as a function of the number of bits of data or check bits the syndrome indicates is in error.

15. The method of claim 12 wherein the delay is a function of the number of bits of data or check bits the syndrome indicates is in error.

16. The method of claim 11 wherein the act of writing any corrected data to the DRAM device comprises:

combining the corrected data with check bits to provide a corrected ECC; and

writing the corrected ECC to the DRAM device.

17. The method of claim 11 wherein the act of writing any corrected data to the DRAM device comprises:

writing the corrected data to a first location in the DRAM device; and

writing the check bits to a second location in the DRAM device that is separate from the first location.

18. The method of claim 11 wherein the act of reading each set of data bits and corresponding sets of check bits from the memory cells after a delay comprises:

after the delay, reading at least one set of data bits and corresponding sets of check bits from a single row of memory cells in the DRAM device; and

waiting until after another of the delays before reading at least one set of data bits and corresponding sets of check bits from a single row of memory cells in the DRAM device.

19. The method of claim 11 wherein the act of reading each set of data bits and corresponding sets of check bits from the memory cells after a delay comprises after the delay, reading at least one set of data bits and corresponding sets of check bits from a plurality of rows of memory cells in the DRAM device before waiting for another of the delays.

20. A scrubbing controller for operating a dynamic random access memory ("DRAM") device, comprising:

an error correcting code ("ECC") generator/checker coupled to a data bus of the DRAM device, the ECC generator/checker being operable to determine if an ECC applied to the ECC generator/checker through the data bus contains at least one error, and, if so, to generate a corrected ECC;

an addressing device coupled to an address bus of the DRAM device, the addressing device generating a sequence of row addresses for the DRAM device;

a control device coupled to a control bus of the DRAM device, the control device being operable to cause data to be written to and read from the DRAM device at an address corresponding to a row address generated by the addressing device; and

a timer triggering the control device to cause at least one ECC to be read from the DRAM device after a delay period, and, if the ECC generator/checker determines that the read ECC contains at least one error, to write to the DRAM device a corresponding corrected ECC generated by the ECC generator/checker, the delay period established by the timer being longer than a period required to refresh memory cells of the DRAM device without generating any errors.

21. The scrubbing controller of claim 20 wherein the ECC generator/checker further comprises a check bit bus coupled to a check bit bus of the DRAM device, the ECC generator/checker coupling check bits of the ECC to and from the DRAM device through the check bit bus and coupling data bits of the ECC to and from the DRAM device through the data bus.

22. The scrubbing controller of claim 20 wherein the delay period established by the timer comprises a function of the temperature of the DRAM device.

23. The scrubbing controller of claim 20 wherein the delay period established by the timer initially comprises a function of the temperature of the DRAM device and is thereafter a function of the errors in at least one read ECC.

24. The scrubbing controller of claim 20 wherein the delay period established by the timer comprises a function of the errors in at least one read ECC.

25. The scrubbing controller of claim 20 wherein the addressing device comprises a counter incrementing from an initial count to a final count corresponding to the memory capacity of the DRAM device.

26. The scrubbing controller of claim 20 wherein the timer comprises:

a register storing a time constant corresponding to the duration of the delay period; and

a periodically incremented counter generating a trigger signal to trigger the control device responsive to reaching a predetermined count, the counter being coupled to the register to load a count corresponding to the time constant prior to the start of the delay period.

27. The scrubbing controller of claim 26 wherein the time constant corresponds to the temperature of the DRAM device.

28. The scrubbing controller of claim 26 wherein the time constant initially corresponds to the temperature of the DRAM device and thereafter corresponds to the number of errors in at least one read ECC.

29. The scrubbing controller of claim 26 wherein the time constant corresponds to the number of errors in at least one read ECC.

30. A computer system, comprising:

a central processing unit ("CPU");

a dynamic random access memory ("DRAM ") device having a data bus, an address bus, and a control bus;

a system controller coupled to the CPU, the system controller including a memory controller coupled to the DRAM device through the data bus, address bus and control bus; and

a scrubbing controller coupled to the DRAM device through the data bus, address bus and control bus, the scrubbing controller comprising:

an error correcting code ("ECC") generator/checker coupled to a data bus of the DRAM device, the ECC generator/checker being operable to determine if an ECC applied to the ECC generator/checker through the data bus contains at least one error, and, if so, to generate a corrected ECC;

an addressing device coupled to an address bus of the DRAM device, the addressing device generating a sequence of row addresses for the DRAM device;

a control device coupled to a control bus of the DRAM device, the control device being operable to cause data to be written to and read from the DRAM device at an address corresponding to a row address generated by the addressing device; and

a timer triggering the control device to cause at least one ECC to be read from the DRAM device after a delay period, and, if the ECC generator/checker determines that the read ECC contains at least one error, to write to the DRAM device a corresponding corrected ECC generated by the ECC generator/checker, the delay

period established by the timer being longer than a period required to refresh memory cells of the DRAM device without generating any errors.

31. The computer system of claim 30 wherein the DRAM device further comprises a check bit bus, and the ECC generator/checker further comprises a check bit bus coupled to the check bit bus of the DRAM device, the ECC generator/checker coupling check bits of the ECC to and from the DRAM device through the check bit bus and coupling data bits of the ECC to and from the DRAM device through the data bus.

32. The computer system of claim 30 wherein the computer system further comprises a temperature sensor coupled to the DRAM device to measure the temperature of the DRAM device, and wherein the scrubbing controller is coupled to the temperature sensor to receive a signal from the temperature sensor indicative of the temperature of the DRAM device, the timer being operable to establish the delay period as a function of the temperature of the DRAM device.

33. The computer system of claim 30 wherein the delay period established by the timer comprises a function of the errors in at least one read ECC.

34. The computer system of claim 30 wherein the addressing device comprises a counter incrementing from an initial count to a final count corresponding to the memory capacity of the DRAM device.

35. The computer system of claim 30 wherein the timer comprises:

a register storing a time constant corresponding to the duration of the delay period; and

a periodically incremented counter generating a trigger signal to trigger the control device responsive to reaching a predetermined count, the counter being coupled to the register to load a count corresponding to the time constant prior to the start of the delay period.

36. The computer system of claim 35 wherein the time constant corresponds to the temperature of the DRAM device.

37. The computer system of claim 35 wherein the time constant initially corresponds to the temperature of the DRAM device and thereafter corresponds to the number of errors in at least one read ECC.

38. The computer system of claim 35 wherein the time constant corresponds to the number of errors in at least one read ECC.

39. The computer system of claim 35 wherein the a scrubbing controller is packaged within the systems controller.

40. The computer system of claim 35 wherein the a scrubbing controller is packaged within the DRAM device.

41. A dynamic random access memory ("DRAM") device, comprising:

an array of memory cells arranged in rows and columns;

an addressing circuit receiving and decoding an external address;

a data path coupling data between a data bus and memory cells corresponding to the decoded memory address;

a command decoder receiving and decoding external memory commands, the command decoder generating control signals for controlling the operation of the DRAM device; and

a scrubbing controller comprising:

an error correcting code ("ECC") generator/checker coupled to a data path of the DRAM device, the ECC generator/checker being operable to determine if an ECC applied to the ECC generator/checker through the data path contains at least one error, and, if so, to generate a corrected ECC;

an addressing generator generating a sequence of row addresses for the DRAM device;

a control device operable to cause data to be written to and read from the DRAM device at an address corresponding to a row address generated by the addressing device; and

a timer triggering the control device to cause at least one ECC to be read from the DRAM device after a first delay period, and, if the ECC generator/checker determines that the read ECC contains at least one error, to write to the memory array a corresponding corrected ECC generated by the ECC generator/checker, the first delay period established by the timer being longer than a period required to refresh the memory cells of the DRAM device without generating any errors.

42. The DRAM device of claim 41, further comprising a refresh controller to refresh the memory cells of the array after a second delay period that is substantially shorter than the first delay period.

43. The DRAM device of claim 42 wherein the command decoder causes the DRAM device to operate in either a normal operating mode or a power-saving mode, and wherein, in the normal operating mode, the refresh controller refreshes the memory cells at a rate corresponding to the second delay period and, in the power-saving mode, the scrubbing controller causes each ECC to be read from the memory array and, in the event of an error, a corrected ECC to be generated an written to the memory array, at a rate corresponding to the first delay period.

44. The DRAM device of claim 41 wherein the ECC generator/checker further comprises a check bit bus coupled to the array of the DRAM device, the ECC generator/checker coupling check bits of the ECC to and from the array through the check bit bus and coupling data bits of the ECC to and from the array through the data path.

45. The DRAM device of claim 41 wherein the timer is operable to establish the delay period as a function of the temperature of the DRAM device.

46. The DRAM device of claim 41 wherein the timer is operable to initially establish the delay period as a function of the temperature of the DRAM device and to thereafter establish the delay period as a function of the errors in at least one read ECC.

47. The DRAM device of claim 41 wherein the delay period established by the timer comprises a function of the errors in at least one read ECC.

48. The DRAM device of claim 41 wherein the addressing device comprises a counter incrementing from an initial count to a final count corresponding to the memory capacity of the DRAM device.

49. The DRAM device of claim 41 wherein the timer comprises:

a register storing a time constant corresponding to the duration of the delay period; and

a periodically incremented counter generating a trigger signal to trigger the control device responsive to reaching a predetermined count, the counter being coupled to the register to load a count corresponding to the time constant prior to the start of the delay period.

50. The DRAM device of claim 49 wherein the time constant corresponds to the temperature of the DRAM device.

51. The DRAM device of claim 49 wherein the time constant initially corresponds to the temperature of the DRAM device and thereafter corresponds to the number of errors in at least one read ECC.

52. The DRAM device of claim 49 wherein the time constant corresponds to the number of errors in at least one read ECC.